SESSION 10 – TAPA I
Analog/RF Devices I

Wednesday, June 16, 10:20 a.m.
Chairpersons: B. Zhao, Skyworks Solution
T. Dan, Sanyo Electric

**10.1 — 10:20 a.m.**
**Three-Dimensional Circuit Integration Based on Self-Synchronized RF-Interconnect Using Capacitive Coupling,** Q. Gu, Z. Xu*, J. Kim, J. Ko and M.F. Chang, University of California, Los Angeles, CA, *G-Plus, Inc., Santa Monica, CA

A self-synchronized RF-interconnect (SSRFI), based on capacitive coupling and peak signal detection, has been successfully demonstrated in 0.18mm CMOS. This SSRFI can be used effectively for vertical interconnects in future 3D IC with small coupling capacitors of 60fF (8x8mm2). This SSRFI is measured with transmission/receiving PRBS data rate of 3Gbit/s and 1.2x10-10 BER. The measured rms jitter value is 1.28ps. The core circuit burns about 4mW from a 1.8V supply and occupies 0.02mm2 chip area.

**10.2 — 10:45 a.m.**
**A 243-GHz $F_T$ and 208-GHz $F_{max}$, 90-nm SOI CMOS SoC Technology with Low-Power Millimeter-Wave Digital and RF Circuit Capability,** N. Zamdmer, J. Kim, R. Trzcinski, J.-O. Plouchart, S. Narasimha, M. Khare, L. Wagner and S. Chaloux, IBM SRDC, Hopewell Junction, NY

A 90-nm SOI CMOS SoC integrates high-performance FETs with 243-GHz Ft, 208-GHzFmax, 1.45-mS/um gm, and sub 1.1-dB NFmin up to 26-GHz. Inductor Q of 20,VNCAP of 1.8-fF/um2, varactor with tuning range as high as 25:1, and low-loss microstrip transmission lines were successfully integrated without extra masks and processing steps. SOI and its low- parasitic junction capacitance enables this high level of performance and will expand the use of CMOS for millimeter-wave applications.

**10.3 — 11:10 a.m.**
**Integration of a 90nm RF CMOS Technology (200GHz $f_{max}$ - 150GHz $f_T$ NMOS) Demonstrated by a 5GHz LNA,** W. Jeamsaksiri, A. Mercha, J. Ramos, D. Linten*, S. Thijs, S. Jenei, C. Detcheverry**, P. Wambacq, R. Velghe** and S. Decoutere, IMEC, Leuven, Belgium, *Vrije Universiteit Brussel, **Philips Research Leuven, Belgium

RF-NMOS with both high fT (150GHz) and fmax (200GHz) presenting a ratio power gain/current gain higher than 1 up to the maximum measurement frequency and a portfolio of high Q passive components have been successfully integrated in a90nm CMOS technology providing a solution for CMOS based RF applications. This achievement is illustrated for the first time by the excellent RF performances in terms of gain, noise figure and power consumption of a 5GHz LNA.

**10.4 — 11:35 a.m.**
**Impact of Mechanical Stress Engineering on Flicker Noise Characteristics,** S. Maeda, Y.-S. Jin, J.-A. Choi, S.-Y. Oh, H.-W. Lee, J.-Y. Yoo, M.-C. Sun, J.-H. Ku, K. Lee, S.-G. Bae, S.-G. Kang, J.-H. Yang, Y.-W. Kim and K.-P. Suh, Samsung Electronics Co., Ltd., Kyoungi-Do, Korea

Relationship between mechanical stress engineering and flicker noise are clarified for the first time using a 50nm level CMOS technology. It is found that enhanced mechanical stress degrades flicker noise characteristics. Trap states and dipoles generated by the stress are considered to be the cause of degradation. It is suggested that the stress engineering is not always the best way to improve transistor performance when considering noise. As a countermeasure, gate dielectric optimization is demonstrated.